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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/752,123	12/29/2000	Calvin Guey	JCLA6706	8730

7590 05/05/2004

J.C. PATENTS INC.
4 VENTURE
SUITE 250
IRVINE, CA 92618

EXAMINER	
GOLE, AMOL V	
ART UNIT	**PAPER NUMBER**
2183	8

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/752,123	GUEY ET AL.	
	Examiner	Art Unit	
	Amol V. Gole	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2, 4, 6, 8, 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 2, 4, 6, 8, 9-12 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file:

#6: Declaration (2/17/04)

#3: Amdt. A (2/17/04)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims **2, 4, 6, 8, 9-12** are rejected under 35 U.S.C. 102(b) as being anticipated by York et al. (US006002881A).

5. In regard to claim 2:

6. York et al. disclose an apparatus for coprocessor data access control (col. 1, line 65), comprising

a central processing unit, for executing central processing unit instructions to perform data processing, wherein the central processing unit instructions includes a plurality of coprocessor memory access instructions (col. 1, lines 66-67; col. 2, lines 1-2);

a memory unit, coupled to the central processing unit, for storing data words (col. 2, lines 3-4) ; and

a coprocessor, coupled to the central processing unit and the memory unit, for accessing and processing the data words stored in the memory unit by one of addressing modes under control of the coprocessor memory access instructions executed by the central processing unit (col. 2, lines 5-10), wherein

the coprocessor memory access instruction having an indicating field (portion of addressing mode information, col. 2, line 15; col. 63, 64, lines 10-20 bits 0-15), and data words are accessed to or from the memory unit by the coprocessor according to the value of the indicating field (to control how many data words are transferred between said memory, col. 2, lines 15-20; also col. 63-64 lines 25-27: the value of bits 0-7 of the indicating field disclose the number of registers to be transferred and the bits 12-15 indicate the first register to be transferred. Hence the value of the indicating field changed by these sub-fields indicates the data words to be accessed to or from the memory unit by the coprocessor).

wherein the indicating field of the coprocessor memory access instruction includes a coprocessor number field (col. 63-64, lines 10-20, bits 8-11), for storing information about a specific coprocessor to be activated (bits 8-11 store the number of the coprocessor i.e. in this case pic_1).

7. Although, York et al. mention that data words are accessed to or from the memory unit by the coprocessor, they are silent on how many data words are accessed. However, it would be deemed inherent to the York et al. apparatus to access N data words where N is a value greater than or equal to 1. The objective of the apparatus of accessing data words would not be met if no data words accessed, i.e. N is equal to 0. Hence, if N data words are transferred, N must be a value greater than or equal to 1.

8. In regard to claim 4:

9. York et al. disclose the apparatus for coprocessor data access control as claimed in claim 2, wherein the indicating field of the coprocessor memory access instruction includes a coprocessor register field, wherein the coprocessor register field is used for storing information about specific registers to be used in the data processing (col. 63-64, lines 10-27: the field of bits 12-15 indicate the first register of the pic_1 <Rlist> and the field of bits 0-7 indicate the number of register to be transferred. Hence the register field comprises of bits 0-7 and 12-15).

10. In regard to claim 6:

11. York et al. teaches of a coprocessor data access control method (col. 4, line 5), comprising the steps of:

providing an instruction (col. 2, lines 11-12) having an indicating field (portion of addressing mode information, col. 2, line 15; col. 63, 64, lines 10-20 bits 0-15); and

accessing data words to or from a memory unit by a specified coprocessor according to the value in the coprocessor indicating field (to control how many data words are transferred between said memory, col. 2, lines 15-20; also col. 63-64 lines 25-27: the value of bits 0-7 of the indicating field disclose the number of registers to be transferred and the bits 12-15 indicate the first register to be transferred. Hence the value of the indicating field changed by these sub-fields indicates the data words to be accessed to or from the memory unit by the coprocessor),

wherein the indicating field of the coprocessor memory access instruction includes a coprocessor number field (col. 63-64, lines 10-20, bits 8-11), for storing information about a specific coprocessor to be activated (bits 8-11 store the number of the coprocessor i.e. in this case pic_1).

12. Although, York et al. mention that data words are accessed to or from the memory unit by the coprocessor, they are silent on how many data words are accessed. However, it would be deemed inherent to the York et al. apparatus to access N data words where N is a value greater than or equal to 1. The objective of the apparatus of accessing data words would not be met if no data words accessed, i.e. N is equal to 0. Hence, if N data words are transferred, N must be a value greater than or equal to 1.

13. In regard to claim 8:

14. The method for coprocessor data access control as claimed in claim 6, wherein the indicating field of the coprocessor memory access instruction includes a coprocessor register field, wherein the coprocessor register field is used for storing information about specific registers to be used in the data processing (col. 63-64, lines 10-27: the field of bits 12-15 indicate the first register of the pic_1 <Rlist> and the field of bits 0-7 indicate the number of register to be transferred. Hence the register field comprises of bits 0-7 and 12-15).

15. In regard to claim 9:

16. York et al. disclose an instruction format (col. 63, 64, lines 10-20) for a coprocessor data access control, wherein the instruction format includes an indicating field (col. 63, 64, lines 10-20, bits 0-15) so that while the instruction format is read by the computer, a particular coprocessor being used (bits 8-11 store the number of the coprocessor i.e. in this case pic_1) and the number of data words being accessed to or from the memory unit is determined by the value of in the indicating field (col. 63-64 lines 25-27: the value of bits 0-7 of the indicating field disclose the number of registers to be transferred and the bits 12-15 indicate the first register to be transferred. Hence the value of the indicating field changed by these sub-fields indicates the data words to be accessed to or from the memory unit by the coprocessor).

17. Although York does not explicitly mention that the instruction format is recorded on a computer readable medium, it is inherent because as the instruction format is for use by a computer to be read, it must be stored on a computer readable medium.

18. **In regard to claim 10:**

19. York et al. disclose the instruction format of claim 9, wherein the indicating field of the instruction format is a coprocessor number field (col. 63, 64, lines 10-27: bits 0-15 form the indicating field. bits 8-11 indicate the coprocessor number i.e. in this case pic_1. Hence the indicating field is a coprocessor number field because field indicates the coprocessor number).

20. In regard to claim 11:

21. York et al. disclose the instruction format of claim 9, wherein the indicating field of the instruction format is a coprocessor register field (col. 63, 64, lines 10-27: bits 0-15 form the indicating field. bits 12-15 indicate the first register of the pic_1's <Rlist>. Hence the indicating field is a coprocessor register field because field indicates the coprocessor register).

22. In regard to claim 12:

23. York et al. disclose the instruction format of claim 9, wherein the indicating field (col. 63, 64, lines 10-27: bits 0-15 form the indicating field.) of the coprocessor memory access instruction includes a coprocessor number field (bits 8-11) and a coprocessor

register field (bits 0-7, bits 12-15), wherein coprocessor number field is used for storing information about a specific coprocessor to be activated (bits 8-11 store the number of the coprocessor i.e. in this case pic_1 that is addressed), and the coprocessor register field is used for storing information about specific registers to be used in the data processing (col. 63-64, lines 10-27: the field of bits 12-15 indicate the first register of the pic_1 <Rlist> and the field of bits 0-7 indicate the number of registers to be transferred).

Response to Arguments

24. Applicant's arguments, see pg. 9-12, filed 2/17/04, with respect to the rejection(s)of claim(s) 2, 4, 6, 8, 9-12 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of a different interpretation of York et al.

25. The indicating field in a coprocessor instruction format is a field of bits according to which N data words are accessed to or from the memory unit by the coprocessor and this indicating field includes a coprocessor number field (from currently amended claim 2). The claim language does not limit the indicating field from having other fields of bits in it for other purposes. Hence, in a different interpretation of the York et al. reference, the indicating field is the all the bits from 0-15 in col. 63-64, lines 10-27.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amol V. Gole whose telephone number is 703-305-8888. The examiner can normally be reached on 9:00-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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